Technology computer-aided design simulation study for a strained InGaAs channel n-type metal-oxide-semiconductor field-effect transistor with a high-k dielectric oxide layer and a metal gate electrode \(^a\)

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The stress distributions in the InGaAs channel regions of strained InGaAs metal-oxide-semiconductor (MOS) field-effect transistors with high-k dielectric layer, metal gate, and InGaAs alloy source/drain (S/D) stressors were studied with three-dimensional process simulations. It was shown that the geometric effects, such as channel width and length, could impact the achievable transistor performance gains. In this work, high-performance III-V MOS devices were achieved by stressors, such as S/D stressors, with the InGaAs alloy material. The resulting mobility improvement was analyzed by the Monte Carlo simulations. Tensile stress along the transport direction was found to dominate mobility gain while narrower devices (<1 \(\mu\)m), and a decrease of tensile stress along the channel direction contributed to a decrease in mobility gain owing to the decreasing width. This work helps the future III-V-based MOS device design and demonstrates that strain engineering is important for future nanoscale device technology.

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I. INTRODUCTION

High mobility narrow band gap group III-V materials are considered to be strong contenders to replace strained-Si channels for logic applications beyond the 22 nm node.\(^1\)–\(^3\) Recent work on III-V devices\(^2\) suggested that high In-content In\(_{x}\)Ga\(_{1-x}\)As had been investigated as a possible candidate for metal-oxide-semiconductor field-effect transistor (MOSFET) applications. Even though these III-V based materials readily demonstrated high electron mobility in high electron mobility transistors, they were less promising for n-type MOSFETs (NMOSFETs) due to lower electron mobility caused by poor interface engineering for the insulator layer and channel and disadvantages when compared with strained Si.\(^4\) A National University Singapore research group overcame the process issue as mentioned above and demonstrated the world’s first III-V NMOSFET with in situ doped lattice-mismatched source/drain (S/D) stressors.\(^5\) Intentional stresses were introduced into the In\(_{0.53}\)Ga\(_{0.47}\)As device channel using In\(_{0.3}\)Ga\(_{0.7}\)As S/D stressors\(^5\) as seen in a similar idea adopted in strained-Si NMOSFETs with silicon-carbon S/D stressors\(^6\) during the transistor fabrication process. However, the lattice-mismatched In\(_{0.4}\)Ga\(_{0.6}\)As regions also induced stresses in the In\(_{0.53}\)Ga\(_{0.47}\)As channel along the width (transverse) and the vertical directions. This paper presents an analysis via the simulation of the width dependence of the stress components (longitudinal, vertical, and transverse) in the NMOS channel region and its influence on mobility.

A three-dimensional (3D) simulation study\(^7\) on the stress distribution in a strained In\(_{0.53}\)Ga\(_{0.47}\)As channel was performed, and the impact of channel width and channel length on the device performance, such as mobility gain, was explored. In Secs. II and III, the stress simulation, the band structure model, and the mobility calculation used in the work are discussed. In Sec. IV, the results of the study are discussed. A summary is provided in Sec. V.

II. STRESS SIMULATION

The simulated process steps reflected the common practices in the fabrication of stress-engineered transistors. The In\(_{0.53}\)Ga\(_{0.47}\)As/InP wafer had the standard crystallographic orientation with a surface direction of (001) and a channel direction along [110]. The recess depth for the In\(_{0.3}\)Ga\(_{0.7}\)As S/D stressor was 15 nm. The metal gate length was 200 nm and the metal gate height was 70 nm. Simplified 3D and two-dimensional (2D) cross-section NMOS structures, as shown in Fig. 1, are studied in this paper. The In\(_{0.53}\)Ga\(_{0.47}\)As channel was confined by epitaxially grown In\(_{0.3}\)Ga\(_{0.7}\)As in the S/D along the transport (x) direction and by wide-region isolation materials, such as SiO\(_2\), in the transverse (y) direction. The whole structure was built on top of the In\(_{0.53}\)Ga\(_{0.47}\)As/InP substrate, as shown in Fig. 1.

A well-developed process stress simulator, ANSYS,\(^7\) was used to calculate the stress distribution. The stress in the MOSFET channel region induced by the expansion of In\(_{0.5}\)Ga\(_{0.5}\)As was simulated by simultaneously solving equa-
ANSYS simulations. Ref. 5 and the simulation results for strained In$_{0.53}$Ga$_{0.47}$As of the stress simulations, both the experimental data from J. Vac. Sci. Technol. B, Vol. 29, No. 3, May/Jun 2011 presented. Figure 2 from the finite element method strain simulation in Ref. 5. a, the work is in good agreement with those extracted from the finite element method strain simulation in Ref. 5. Figure 2(a) also shows the finite element calculation of vertical strain in the In$_{0.53}$Ga$_{0.47}$As channel region with adjacent In$_{0.4}$Ga$_{0.6}$As S/D stressors. The gate length and the recess depth were from 50 to 400 nm and 15 nm, respectively. Lateral tensile strain was induced in the In$_{0.53}$Ga$_{0.47}$As channel due to its 0.9% lattice mismatch with In$_{0.4}$Ga$_{0.6}$As. This was expected to boost electron mobility. The average strain magnitude in the region where inversion charge flowed, i.e., the top 5 nm, increased as gate length decreased. This indicated the scalability of the S/D stressor technology. In Fig. 2(b), the simulation results of lateral strain and vertical strain as a function of lateral position and depth position are also compared with that in Ref. 9. Note that solid lines are simulation results and symbols are data from Ref. 9.

III. BAND STRUCTURE AND MOBILITY CALCULATION

A. Band structure calculations

The longitudinal tension of the In$_{0.53}$Ga$_{0.47}$As lattice in the channel region broke the symmetry of the band structure which lifted degeneracy at the Γ, X, and L points of the conduction bands. This break in symmetry break also resulted in a decrease in electron effective mass along the transport (x) direction. The conduction band structure of InGaAs was calculated with an empirical pseudopotential method as shown in Fig. 3.

The second derivatives of conduction band with energy $E$ were computed with respect to momentum $k$ from a pseudopotential band structure to determine effective mass and a
nonparabolic shape. Thus, it could be obtained that some important band structure-related parameters could be extracted from the pseudopotential band structures, such as the energies of valley separations, the longitudinal and transverse effective masses, and the nonparabolic shape parameter $\alpha$, which were defined by the following $E$-$k$ dispersion relation:

$$E(k) = \frac{1}{2} \left( \frac{k^2}{m_{L}} + \frac{k^2}{m_{X}} \right),$$

where $k_{L}$ and $k_{X}$ were the components of momentum parallel and transverse to the direction of symmetry, respectively. Based on this equation, $\alpha$ was obtained by averaging in three-dimensional $k$-space. Band structure-related parameters as mentioned above were included in the simulations. The nonparabolic parameters for $\Gamma$, $L$, and $X$-valleys are denoted as $\alpha_{\Gamma}$, $\alpha_{L}$, and $\alpha_{X}$, respectively.

A physical understanding of the origin of the enhancement of InGaAs NMOSFET under stress was obtained by considering a multivalley conduction band model, where the deformation potential values were extracted from the pseudopotential band structure, as mentioned above. The InGaAs conduction band consisted of three predominant valleys $\Gamma$, $L$, and $X$, out of which most of the carriers populate the lowest mass $\Gamma$-valley. Fischetti’s method was followed to deal with the nonparabolic effects for the electron inversion layer system in the simulations. Strain not only affected conduction band edge shift but also increased the nonparabolic parameter. This nonparabolic effect would also cause more electrons to occupy the $\Gamma$-valley under strain condition as compared with the control one owing to a higher nonparabolic parameter, $\alpha_{\Gamma}$, under strain. For the relaxed InGaAs, $\alpha_{L}$ and $\alpha_{X}$ were very small with respect to $\alpha_{\Gamma}$. The band structure calculations show that $\alpha_{\Gamma}$ is larger in strained InGaAs than in relaxed InGaAs, while $\alpha_{L}$ and $\alpha_{X}$ almost remain unchanged.

For bulk InGaAs, conduction band splitting between $\Gamma$ and $L$ bands was relatively large, causing the population of the $L$ valleys to be negligible and all electrons to reside in the $\Gamma$-valley. For the unstrained InGaAs channel NMOS structure under inversion bias conditions, effective electric field caused by gate confined potential in the growth direction. Electrons in the channel became a quasi-2D electron gas, and the population of $L$-valley-type and $X$-valley-type subbands became considerable. Physical insight about the three valley subbands included in the simulation for III-V MOS system under inversion operation can be found in Ref. 12.

### B. Mobility calculation

In previous publications, calculations of the carrier mobility in inversion layers were presented using the Monte Carlo method. Here the results obtained by extending those calculations are presented to include the addition of the Coulomb scatterings due to the high-$k$ dielectric layer and metal gate for the strained InGaAs inversion layer.

In the presence of an interfacial oxide, such as SiON, only the lowest energy TO phonons of the two oxides, SiON, and the high-$k$ oxide, were considered because these modes were the most important ones for mobility degradation. These led to the spin orbit (SO) phonon modes. Using the expressions for these three SO phonon modes and for the corresponding total effective dielectric functions reported in the Appendix in Ref. 17, the scattering rates were evaluated. Nevertheless, in view of the still-debated cause of high-$k$ mobility degradation, the approximations involved in the described SO phonon scattering model, and the experimental uncertainties, some calibration might be necessary.

For electrons, the band structure was approximated using $\Gamma$, $L$, and $X$-valley minima with ellipsoidal equal-energy surfaces, with nonparabolic shape parameter $\alpha$ included in the first order from the pseudopotential band structure results. The confining potential was obtained by solving the self-consistent Schrödinger and Poisson equations. The scatterings due to the acoustic phonons, the optical phonons, and the surface roughness were considered using the standard models. The Coulomb scattering, including the interface trap effect, was treated using the method proposed in Refs. 16 and 18. The scattering rate for polar optical scattering was calculated using the method found in Ref. 19. The scattering rate for piezoelectric scattering was calculated using the approach outlined in Ref. 20. Note that scattering processes such as polar optical scattering, ionized impurity scattering, and piezoelectric scattering are insensitive to strain. The strain effect was included by first performing conduction band structure calculations for strained InGaAs using the pseudopotential method. The resulting energy shifts of the valley minima and the effective masses were used in the approximation of the band structure.

The deformation potentials for various scattering rates can be found in Ref. 18. The strength of the deformation potential of GaAs was lightly modulated to fit the experimental InGaAs mobility data. The electron mobility in strained InGaAs NMOSFET was experimentally extracted at various vertical effective electric fields, $E_{\text{eff}}$, from Ref. 5, as shown in Fig. 4. Universal Si mobility was also included for comparison. The simulated carrier mobility was calculated with the same effective electric field for comparison. The simulated lateral strain resulted in an electron mobility gain of the...
NMOS with an InGaAs S/D stressor and is shown in Fig. 5 as a function of gate length. The simulated results of electron mobility gain in Fig. 5 were extracted with the same gate width but different gate lengths. Note that the mobility gain is defined as the ratio of strained mobility to unstrained mobility. It was found that the increased electron mobility gain in the short gate length device structure was mainly due to the increase in lateral strain $\varepsilon_{xx}$ induced by the InGaAs S/D stressor.

**IV. RESULTS AND DISCUSSIONS**

From the ANSYS simulations, the stress stayed relatively constant in the surface channel region beneath the gate, where the electron transport is most critical. Averaged $S_{xx}$, $S_{yy}$, and $S_{zz}$ in the surface channel versus the transistor width for gate lengths of 50 and 200 nm are both plotted in Fig. 6. The effect of In$_{0.4}$Ga$_{0.6}$As stressors alone was considered on the stress distribution in the NMOSFETs, with the results presented in Fig. 6. As expected, the tendency of In$_{0.4}$Ga$_{0.6}$As alloy stressors to expand in the channel region induced tensile stress along the $x$ direction and compressive stress along the $y$ and $z$ directions. With decreasing transistor width, stress along the $x$ direction, $S_{xx}$, initially remained constant before decreasing slightly, as illustrated in Fig. 6. The constraints imposed by the isolation region and the In$_{0.53}$Ga$_{0.47}$As substrate caused the strain in the $y$ direction to approach zero with increasing width, corresponding to a decrease in stress in the $y$ direction. It was found that $|S_{yy}|$ has a maximum value at $W=0.3$ $\mu$m for NMOS. This is largely attributed to the constraint from the isolation region as the device width shrinks to the limit of the zero width stress boundary condition of $|S_{yy}|$. Therefore, it is natural to see a local maximum of $|S_{yy}|$ appearing before the vanishing channel width. The particular value of $W=0.3$ $\mu$m, where the maximum of $|S_{yy}|$ occurs, actually depends on the specific geometry of the device under consideration. When width increases beyond approximately 3 $\mu$m, all three stress components approach a constant. The primary function of the isolation region is considered to be the provision of isolation. The observed strain effects associated with the isolation region are very minimal because no equivalent intrinsic compressive stresses for the isolation region are simulated. On the other hand, the absolute magnitude of $S_{zz}$ was observed to change slightly with decreasing width for a NMOS with an In$_{0.4}$Ga$_{0.6}$As stressor.

The consequent mobility gain versus width is shown in Fig. 7. There are three different stress elements, as discussed in Fig. 6, included in Fig. 7. Similar to the stress results, the mobility gain also shows considerable width sensitivity. Figure 7 shows the simulated mobility gain as a function of width for the two gate lengths of 50 and 200 nm NMOSFET devices with In$_{0.4}$Ga$_{0.6}$As stressors. Mobility gain was almost unchanged with decreasing width when the width was larger than 1 $\mu$m. In order to understand the contribution of the stress component to mobility gain, each stress component was imported into the Monte Carlo simulator separately; i.e., only one stress component was used in one set of device simulations. It was found that the stress along the channel direction, $S_{xx}$, contributed the most to the improvement while $S_{yy}$ contributed the least. It was also found that ultranarrow $W$ devices have a lower mobility gain. The shrinkage of mobili-
ity gain in the device with $W$ below 1 $\mu$m was mainly due to decreasing the magnitude of $S_{xx}$ with decreasing channel width.

V. CONCLUSIONS

In this study, the stress components in three directions in the In$_{0.53}$Ga$_{0.47}$As channel of NMOSFETs with an In$_{0.4}$Ga$_{0.6}$As alloy source/drain stressor were simulated. The resulting mobility gain was analyzed. Tensile stress along the transport direction was found to dominate mobility gain. However, for NMOSFETs with In$_{0.4}$Ga$_{0.6}$As S/D stressors and a width below 1 $\mu$m, the shrinkage of tensile stress along the channel direction ($S_{xx}$) contributes to the decrease of the mobility gain owing to the decreasing width. In conclusion, 3D stress simulations are necessary to accurately study device performance induced by In$_{0.4}$Ga$_{0.6}$As S/D stressors.

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